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1 Prefetching in supercomputer instruction caches
J. E. Smith, W.-C. Hsu
December 1992 **Proceedings of the 1992 ACM/IEEE conference on Supercomputing**
Full text available: pdf(1.05 MB) Additional Information: full citation, references, citings, index terms

2 Architectural and compiler support for effective instruction prefetching: a cooperative approach
February 2001 **ACM Transactions on Computer Systems (TOCS)**, Volume 19 Issue 1
Full text available: pdf(432.96 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Instruction cache miss latency is becoming an increasingly important performance bottleneck, especially for commercial applications. Although instruction prefetching is an attractive technique for tolerating this latency, we find that existing prefetching schemes are insufficient for modern superscalar processors, since they fail to issue prefetches early enough (particularly for nonsequential accesses). To overcome these limitations, we propose a new instruction prefetching technique where ...

**Keywords**: compiler optimization, instruction prefetching

3 Adaptive data prefetching using cache information
Ando Ki, Alan E. Knowles
July 1997 **Proceedings of the 11th international conference on Supercomputing**
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4 Multithreading I: Pointer cache assisted prefetching
Jamison Collins, Suleyman Sair, Brad Calder, Dean M. Tullsen
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1 Speculative prefetching

Y. Jégou, O. Temam

August 1993 **Proceedings of the 7th international conference on Supercomputing**

Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms

A hardware prefetching mechanism named Speculative Prefetching is proposed. This scheme detects vector accesses issued by a load/store instruction and prefetches the corresponding data. The scheme requires no software add-on, and in some cases it is more powerful than software techniques for identifying regular accesses. The tradeoffs related to its hardware implementation are extensively discussed in order to finely tune the mechanism. Experiments show that average memory ...

2 Memory system analysis and optimization: Compiler orchestrated prefetching via speculation and predication

Rodric M. Rabbah, Hariharan Sandanagobalane, Mongkol Ekpanyapong, Weng-Fai Wong

October 2004 **Proceedings of the 11th international conference on Architectural support for programming languages and operating systems**

Full text available: pdf(247.55 KB) Additional Information: full citation, abstract, references, index terms

This paper introduces a compiler orchestrated prefetching system as a unified framework geared toward ameliorating the gap between processing speeds and memory access latencies. We focus the scope of the optimization on specific subsets of the program dependence graph that succinctly characterize the memory access pattern of both regular array-based applications and irregular pointer-intensive programs. We illustrate how *program embedded precomputation via speculative execution* can accura ...

**Keywords**: precomputation, predicated execution, prefetching, speculation

3 Resource-aware speculative prefetching in wireless networks

N. J. Tuah, M. Kumar, S. Venkatesh

January 2003 **Wireless Networks**, Volume 9 Issue 1

Full text available: pdf(212.89 KB) Additional Information: full citation, abstract, references, index terms

Mobile users connected to wireless networks expect performance comparable to those on wired networks for interactive multimedia applications. Satisfying Quality of Service (QoS) requirements for such applications in wireless networks is a challenging problem due to

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Jamison Collins, Suleyman Sair, Brad Calder, Dean M. Tullsen
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.21 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Data prefetching effectively reduces the negative effects of long load latencies on the performance of modern processors. Hardware prefetchers employ hardware structures to predict future memory addresses based on previous patterns. Thread-based prefetchers use portions of the actual program code to determine future load addresses for prefetching.This paper proposes the use of a pointer cache, which tracks pointer transitions, to aid prefetching. The pointer cache provides, for a given pointer's ...

2 Dynamically allocating processor resources between nearby and distant ILP
Rajeev Balasubramonian, Sandhya Dwarkadas, David H. Albonesi
May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture**, Volume 29 Issue 2
Full text available: pdf(998.02 KB) Additional Information: full citation, abstract, references, citings, index terms

*Modern superscalar processors use wide instruction issue widths and out-of-order execution in order to increase instruction-level parallelism (ILP). Because instructions must be committed in order so as to guarantee precise exceptions, increasing ILP implies increasing the sizes of structures such as the register file, issue queue, and reorder buffer. Simultaneously, cycle time constraints limit the sizes of these structures, resulting in conflicting design requirements.*

*In ...*

3 Software support for speculative loads
Anne Rogers, Kai Li
September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems**, Volume 27 Issue 9
Full text available: pdf(1.33 MB) Additional Information: full citation, references, citings, index terms

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